

**ABSTRACT**

A demodulator for use in a satellite communication system, which is operative for receiving a modulated signal having a data rate  $R$  (i.e., the demodulator receives  $R$  input samples per second). The demodulator includes a demultiplexer circuit having  $N$  shift registers, which functions to receive the  $R$  data samples per second as an input signal. The demultiplexer circuit operates to input the  $R$  input samples sequentially into the  $N$  shift registers such that each of the shift registers receives input samples at a data rate of  $R/N$  samples per second. The demodulator further includes signal recovery circuitry for processing the input samples contained in each of the  $N$  shift registers so as to regenerate the data contained in the incoming modulated signal transmitted by the satellite.